WHAT IS CLAIMED IS:

1. A dynamic random access memory device capable of converting from a full density memory device to a reduced density memory device to compensate for cell failures in a plurality of cell blocks, the memory device comprising:

a row address mapping fuse for selectively determining row address combinations void of cell failures and capable of storing data bits; and

row address mapping logic coupled to the row address mapping fuse for receiving a row address mapping signal from the row address mapping fuse and receiving row address signals and or routing specific data bits to the row address combinations void of cell failures and capable of storing the data bits.

2. The dynamic random access memory device of claim 1, and further comprising:

a reduced density enable signal for switching the memory device between a full density mode and a reduced density mode;

a logic value setting signal;

a multiplexer having a first input coupled to the reduced density enable signal, a second input coupled to the logic value setting signal, and a third input coupled to a row address; and

wherein an output signal of the multiplexer is coupled to an input of the row address mapping logic.

3. The dynamic random access memory device of claim 2, wherein the row address mapping logic receives a plurality of row address signals from a row address multiplexer and the output signal of the multiplexer.

4. The dynamic random access memory device of claim 2, wherein the output signal of the multiplexer is the logic value setting signal when the memory device is operating in the reduced density mode.

5. The dynamic random access memory device of claim 2, wherein the output signal of the multiplexer is the row address when the memory device is operating in the full density mode.

6. The dynamic random access memory device of claim 2, and further comprising:

a plurality of row address mapping fuses;

a plurality of row address mapping logics;

a plurality of bank cell arrays; and

wherein an output of each row address mapping logic is coupled to a corresponding input of a bank cell array such that data bits may be routed to row address combinations void of cell failures and capable of storing the data bits within the particular bank cell array independent of other bank cell arrays.

7. The dynamic random access memory device of claim 2, wherein the row address mapping logic utilizes a selection table defining selected locations void of cell failures and capable of storing the data bits.

8. A method of converting a full density memory device to a reduced density memory device, the method comprising:

selectively determining a reduced density address combination having addresses which omit cell blocks having cell block failures; and

storing data bits at an address within the reduced density address combination.

9. The method of claim 8, and further comprising:

switching the memory device between a full density mode and a reduced density mode.

10. The method of claim 8, wherein the step of storing data bits further comprises:

replacing a row address signal with a logic value signal such that a data bit is stored at a cell block void of errors.

11. The method of claim 8, wherein the step of selectively determining a reduced density address combination further comprises:

selectively determining a plurality of addresses which avoid cell blocks having cell block failures.

12. The method of claim 8, wherein the step of selectively determining a reduced density address combination further comprises:

defining selected locations of a cell block array to which information may be stored without error.

13. The method of claim 8, wherein the step of selectively determining a reduced density address combination further comprises:

selectively determining a reduced density address combination based upon a row address mapping signal in combination with a logic value signal.

14. A memory device capable of converting from a full density memory device to a reduced density memory device to compensate for cell failures in a plurality of cell blocks, the memory device comprising:

means for determining address combinations capable of storing data bits and void of cell block failures; and

means for routing data bits to the address combinations capable of storing the data bits.

15. The memory device of claim 14, and further comprising:

means for switching the memory device between a full density mode and a reduced density mode.

16. The memory device of claim 14, and further comprising:

means for replacing an address register signal with a logic value signal.

17. The memory device of claim 14, wherein the means for determining address combinations further comprises:

means for selectively determining address combinations capable of storing data bits based upon a mapping truth table.

18. A dynamic random access memory device capable of converting from a full density memory device to a half density memory device to compensate for cell failures in a plurality of cell blocks, the memory device comprising:

control logic;

a command decoder for bank active, precharge, read and write commands;

a plurality of address registers;

a row address counter;

a row address multiplexer having an input coupled to an output of the row address counter and having a plurality of inputs coupled to the plurality of address registers for receiving a plurality of address signals;

a bank control logic having an input coupled to the control logic and having an input coupled to a bank address register for receiving a bank address signal;

a half density enable fuse for providing a half density enable signal for switching the memory device between a full density mode and a half density mode;

a logic value setting fuse for providing a logic value setting signal;

a multiplexer having a first input coupled to an output of the row address multiplexer, a second input coupled to an output of the logic value setting fuse for receiving the logic value setting signal, and a third input coupled to an output of the half density enable fuse for receiving the half density enable signal;

a row address mapping fuse for providing selectively determining address combinations void of cell failures and for providing a row address mapping signal;

row address mapping logic having a first input coupled to an output of the row address mapping fuse for receiving the row address mapping signal, a second input coupled to the output of the multiplexer, and a plurality of inputs electrically coupled to a plurality of outputs of the row address multiplexer;

a bank row address latch and decoder having a first input coupled to an output of the row address mapping logic and having a second input coupled to an output of the bank control logic; and

a bank cell array having an input coupled to an output of the bank row address latch and decoder.